IN THE CLAIMS

1. (currently amended) A method of fabricating a memory cell, comprising:
forming a silicide layer on a word line of the memory cell concurrently with forming a silicide layer on a contact to a source/drain region of the memory cell[[.]];
wherein the silicide layer formed on the word line is not limited by a width of the contact.

2. (original) The method of claim 1, wherein forming a silicide layer comprises forming a self-aligned silicide layer.

3. (original) The method of claim 1, wherein forming a silicide layer further comprises forming a layer of silicide selected from the group consisting of chromium silicide, cobalt silicide, hafnium silicide, molybdenum silicide, niobium silicide, tantalum silicide, titanium silicide, tungsten silicide, vanadium silicide and zirconium silicide.

4. (original) The method of claim 1, wherein forming a silicide layer further comprises forming a layer of silicide selected from the group consisting of titanium silicide and cobalt silicide.

5. (original) The method of claim 1, further comprising forming the silicide layer on the word line of the memory cell concurrently with forming a silicide layer on a contact to each of a drain region of the memory cell and a source region of the memory cell.

6. (currently amended) A method of fabricating an array of floating-gate memory cells, comprising:
forming a layer of silicide on exposed portions of one or more word lines of the array, each word line extending to a plurality of columns of the array;
while forming the layer of silicide on the exposed portions of the one or more word lines, forming a layer of silicide on one or more contacts to drain regions of the memory cells; and

while forming the layer of silicide on the exposed portions of the one or more word lines, forming a layer of silicide on one or more interconnects to source regions of the memory cells, wherein each interconnect contacts source regions of memory cells of one or more columns of the array[[.]];

wherein the exposed portions of the one or more word lines are independent of the contacts and interconnects.

7. (original) The method of claim 6, wherein each interconnect contacts source regions to memory cells of the same number of columns as an associated word line.

8. (currently amended) The method of claim 6, wherein forming the layer of silicide on the exposed portions of the one or more word lines of the array, forming the layer of silicide on the one or more contacts to drain regions of the memory cells and forming the layer of silicide on the one or more interconnects to source regions of the memory cells further comprises:

forming a layer of refractory metal on the exposed portions of the word lines, contacts to drain regions, interconnects to source regions and interposing structures;

reacting the refractory metal with free silicon in the word lines, contacts to drain regions and interconnects to source regions; and

removing unreacted refractory metal from the interposing structures.

9. (original) The method of claim 8, wherein forming the layer of refractory metal further comprises forming a layer of refractory metal selected from the group consisting of chromium, cobalt, hafnium, molybdenum, niobium, tantalum, titanium, tungsten, vanadium and zirconium.

10. (original) The method of claim 8, wherein forming the layer of refractory metal further comprises forming a layer containing cobalt or titanium.

11. (original) A method of forming a floating-gate memory cell, comprising:

forming a word line stack, comprising:

forming a tunnel dielectric layer overlying a semiconductor substrate;

forming a floating-gate layer overlying the tunnel dielectric layer;

forming an intergate dielectric layer overlying the floating-gate layer;

forming a polysilicon control gate layer overlying the intergate dielectric layer; and

forming a sacrificial cap layer overlying the polysilicon control gate layer;

forming dielectric spacers on sidewalls of the word line stack;

forming a drain region in the substrate on a first side of the word line stack;

forming a source region in the substrate on a second side of the word line stack;

forming a first polysilicon contact to the source region;

removing the cap layer, thereby exposing the polysilicon control gate layer; and

forming silicide layers concurrently on the polysilicon control gate layer and the first polysilicon contact.

12. (original) The method of claim 11, wherein the drain and source regions are formed after forming the word line stack.

13. (original) The method of claim 11, wherein:

forming the sacrificial cap layer further comprises forming the sacrificial cap layer of a first dielectric material; and

forming the dielectric spacers further comprises forming the dielectric spacers of a second dielectric material different from the first dielectric material.

14. (original) The method of claim 11, wherein forming the first polysilicon contact further comprises:

forming an insulator layer overlying the word line stack, the drain region and the source region;

removing a first portion of the insulator layer to expose the cap layer;

removing a second portion of the insulator layer to expose the source region;

forming a polysilicon layer in contact with the source region.

15. (original) The method of claim 14, wherein removing the first portion of the insulator further comprises planarizing the insulator layer using the cap layer as a stop layer.

16. (original) The method of claim 15, wherein removing the second portion of the insulator layer further comprises forming a mask overlying the planarized insulator layer to expose portions of the insulator layer to be removed and etching the exposed portions of the insulator layer to expose the source region.

17. (original) The method of claim 11, further comprising:
forming a second polysilicon contact to the drain region; and
forming silicide layers concurrently on the polysilicon control gate layer, the first polysilicon contact and the second polysilicon contact.

18. (original) The method of claim 17, wherein forming the first polysilicon contact and forming the second polysilicon contact further comprises:
forming an insulator layer overlying the word line stack, the drain region and the source region;
removing a first portion of the insulator layer to expose the cap layer;
removing a second portion of the insulator layer as a contact hole to expose the drain region;
removing a third portion of the insulator layer as a trench to expose the source region;
forming a polysilicon layer filling the contact hole and the trench.

19. (original) The method of claim 18, wherein forming the polysilicon layer further comprises forming a blanket layer of polysilicon and planarizing the blanket layer of polysilicon using the cap layer as a stop layer.

20. (original) The method of claim 11, wherein:
forming the sacrificial cap layer further comprises forming the sacrificial cap layer of a first dielectric material; and

forming the dielectric spacers further comprises forming the dielectric spacers of a second dielectric material different from the first dielectric material.

21. (original) A method of forming an array of floating-gate memory cells, comprising:
forming a first dielectric layer on a silicon substrate;
forming a first polysilicon layer on the first dielectric layer;
forming a second dielectric layer on the first polysilicon layer;
forming a second polysilicon layer on the second dielectric layer;
forming a third dielectric layer on the second polysilicon layer;
patterning the first dielectric layer, the first polysilicon layer, the second dielectric layer, the second polysilicon layer and the third dielectric layer to define word line stacks;
forming source and drain regions between adjacent word line stacks;
forming dielectric spacers on sidewalls of the word line stacks;
forming an insulator layer between adjacent word line stacks;
removing a portion of the insulator layer to define contact holes exposing drain regions and trenches exposing source regions, wherein each contact hole exposes one drain region and wherein each trench exposes a plurality of source regions;
filling the contact holes and trenches with a third polysilicon layer;
removing the third dielectric layer, thereby exposing the second polysilicon layer;
forming a silicide layer on the second polysilicon layer; and
forming a silicide layer on the third polysilicon layer.

22. (currently amended) The method of claim 21, wherein forming the source and drain regions occurs prior to patterning the ~~layers~~ first dielectric layer, the first polysilicon layer, the second dielectric layer, the second polysilicon layer and the third dielectric layer.

23. (original) The method of claim 21, wherein the third dielectric layer, the dielectric spacers and the insulator layer each contain a different dielectric material.

24. (original) The method of claim 23, wherein the third dielectric layer comprises a silicon nitride, the dielectric spacers comprise tetraethylorthosilicate and the insulator layer comprises a doped silicate glass.

25. (original) The method of claim 24, wherein the doped silicate glass comprises borophosphosilicate glass.

26. (original) The method of claim 21, wherein forming the silicide layer on the second polysilicon layer occurs concurrently with forming the silicide layer on the third polysilicon layer.

27. (original) The method of claim 21, wherein forming the silicide layer on the second polysilicon layer and forming the silicide layer on the third polysilicon layer further comprise forming a self-aligned silicide layer on the second and third polysilicon layers.

28. (original) The method of claim 27, wherein forming the self-aligned silicide layer on the second and third polysilicon layers further comprises forming a self-aligned silicide layer using a refractory metal selected from the group consisting of chromium, cobalt, hafnium, molybdenum, niobium, tantalum, titanium, tungsten, vanadium and zirconium.

29. (original) The method of claim 27, wherein forming the self-aligned silicide layer on the second and third polysilicon layers further comprises forming a self-aligned silicide layer using a refractory metal selected from the group consisting of cobalt and titanium.

30. (original) The method of claim 21, wherein removing a portion of the insulator layer to define trenches exposing source regions further comprises exposing source regions along an entire length of a word line stack.

31. (original) The method of claim 21, further comprising:
forming a bit line coupled to drain regions of a column of memory cells, wherein the bit line is individually coupled to each drain region of the column of memory cells;

forming at least one contact to a word line stack of a row of memory cells; and

forming at least one contact to source regions of the row of memory cells.

32. (original) The method of claim 31, further comprising:

forming only one contact to the word line stack of the row of memory cells; and

forming only one contact to the source regions of the row of memory cells.

33-49 (Cancelled)